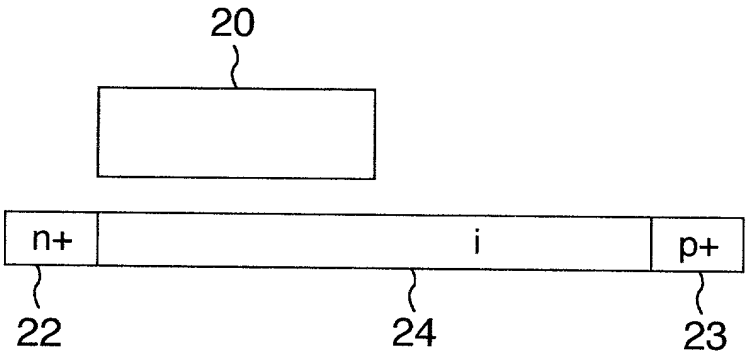
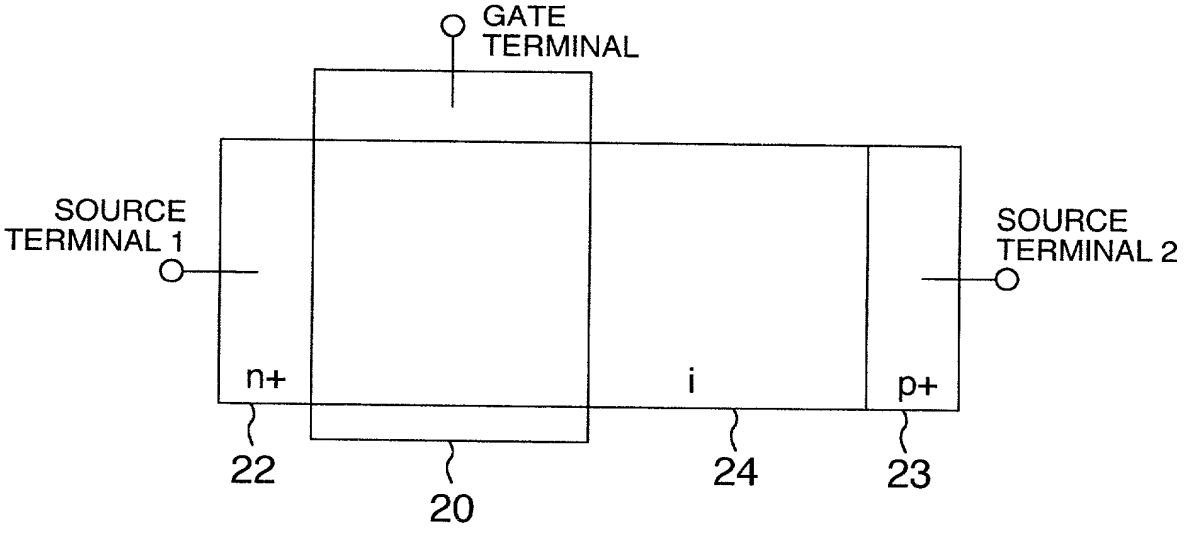
FIG.1A



CROSS SECTION

FIG.1B



PLAN VIEW

FIG.2

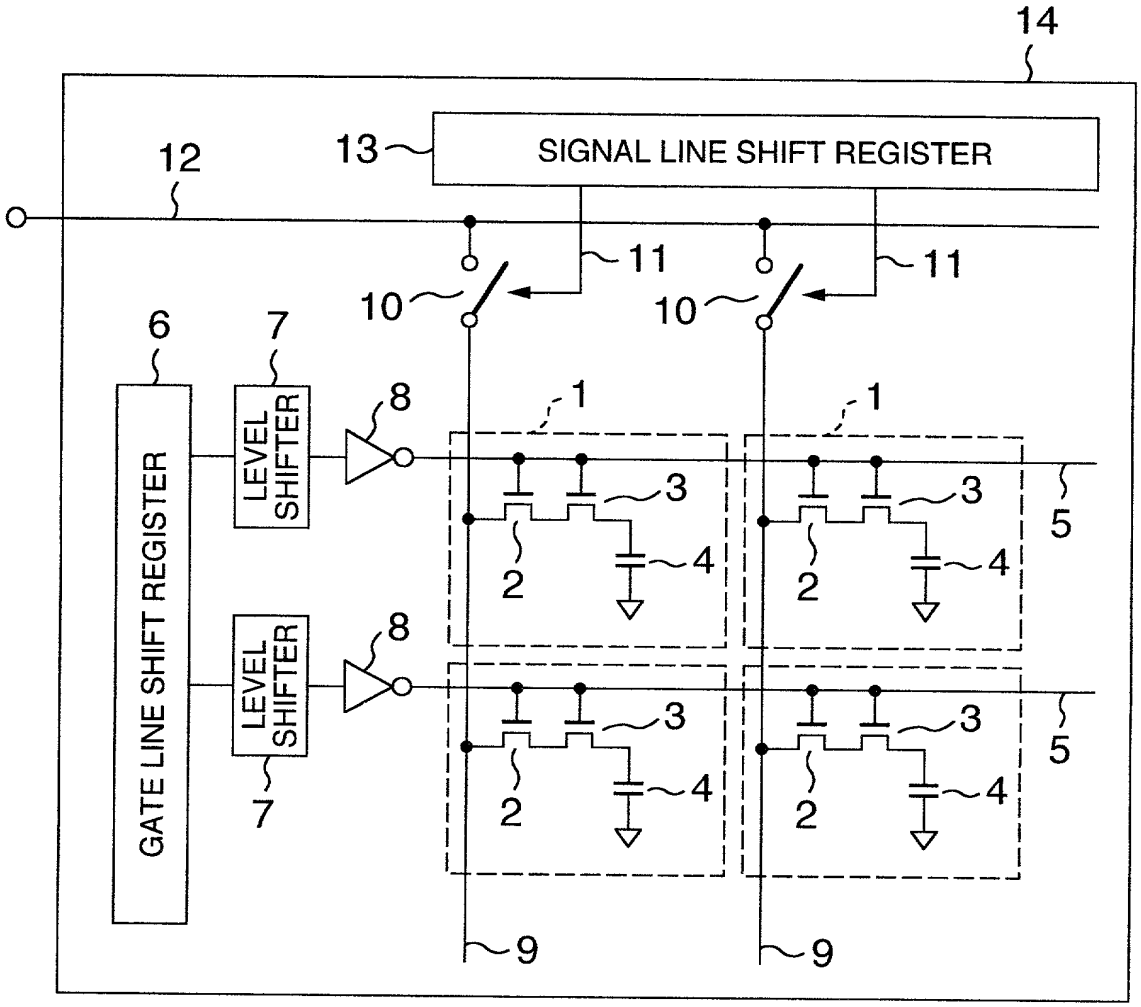

14
12
13
SIGNAL LINE SHIFT REGISTER
11
11
10
10
6
7
GATE LINE SHIFT REGISTER
LEVEL SHIFTER
LEVEL SHIFTER
8
8
7
1
1
2
3
4
5
9
9

FIG.3A

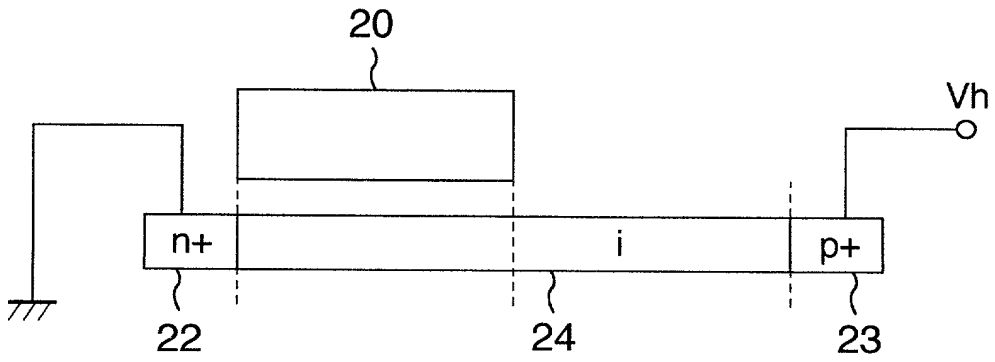


FIG.3B

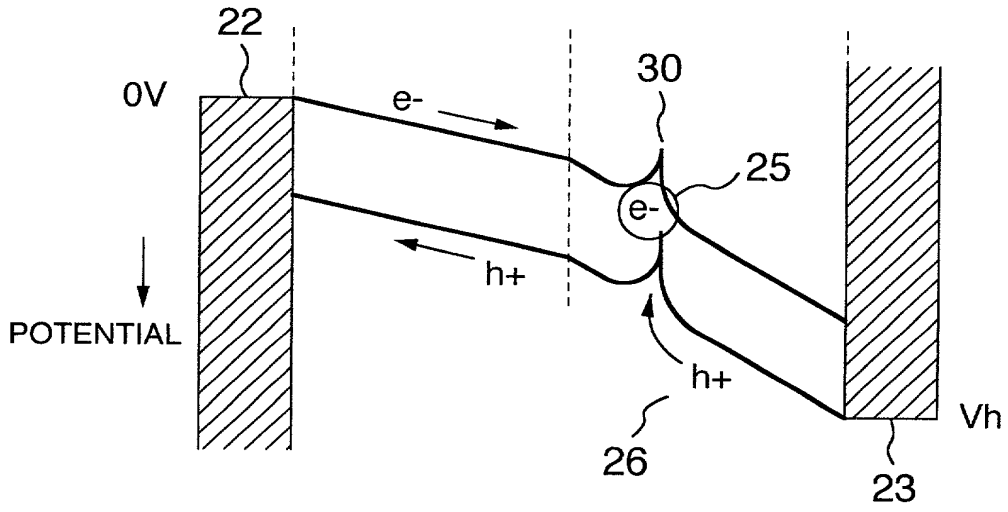


FIG.3C

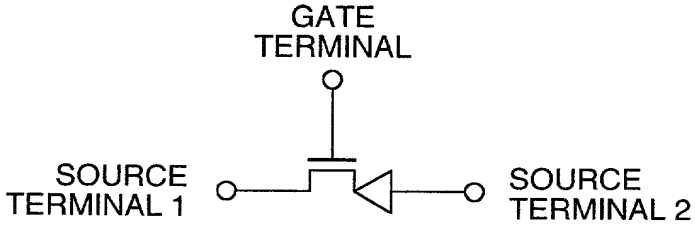
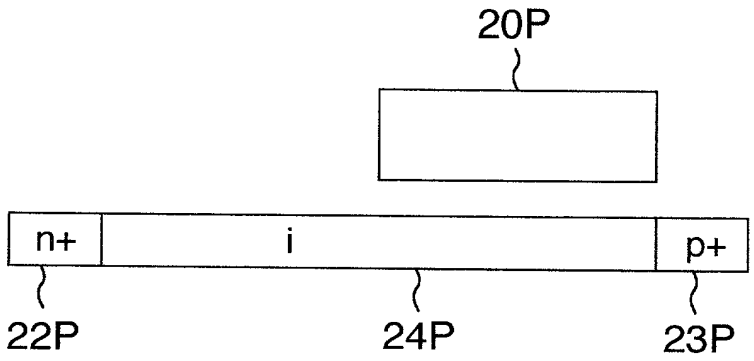
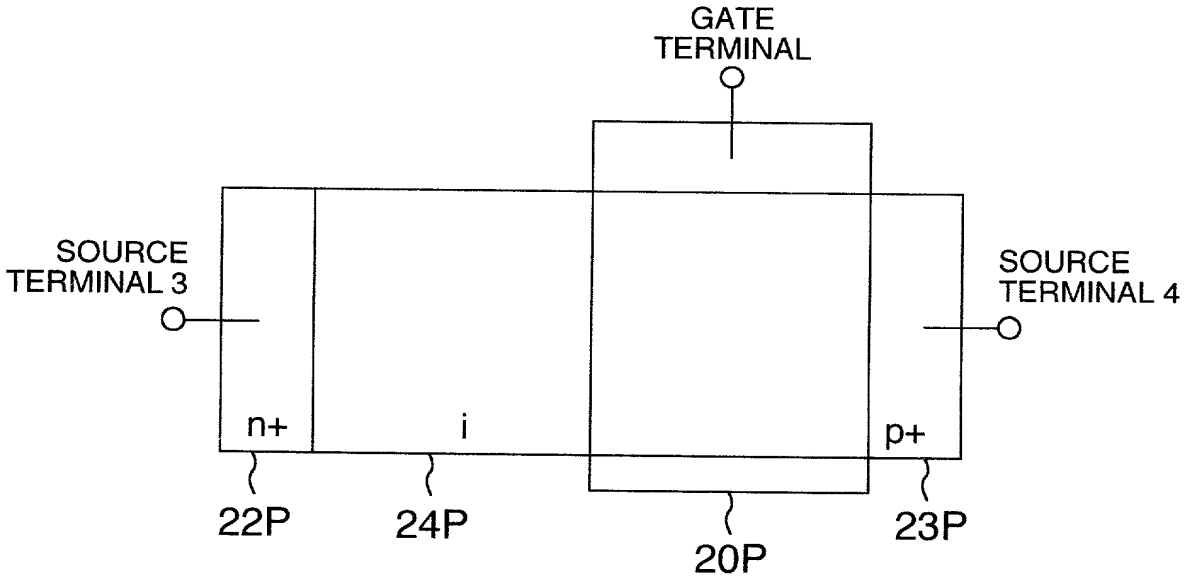


FIG.4A



CROSS SECTION

FIG.4B



PLAN VIEW

FIG.4C

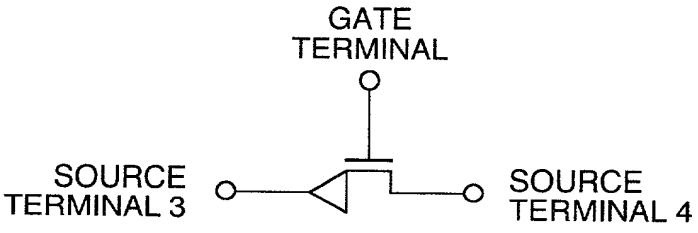


FIG.5

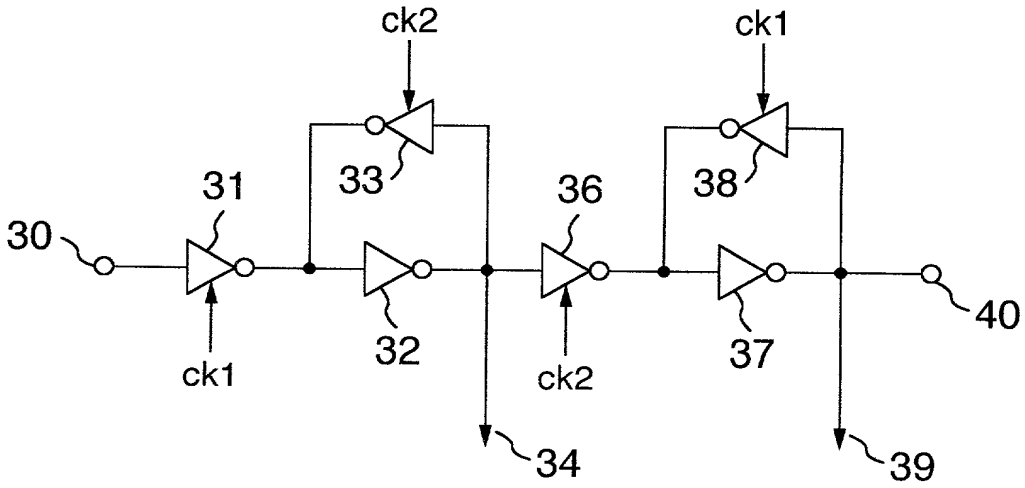


FIG.6

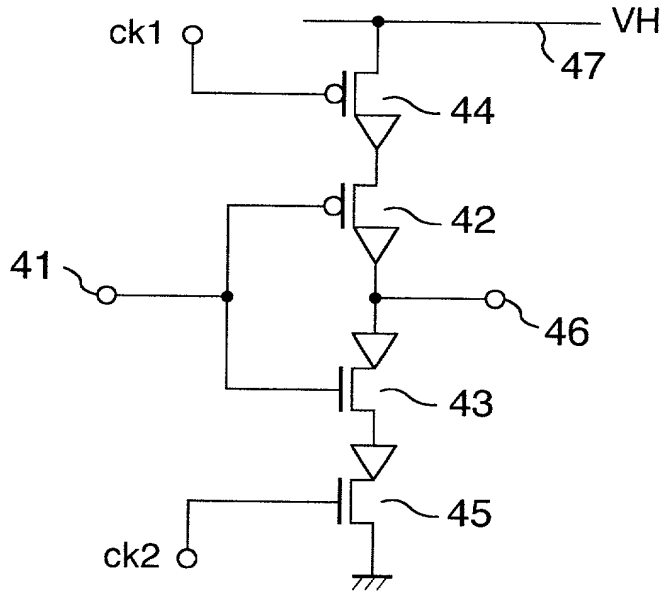


FIG.7

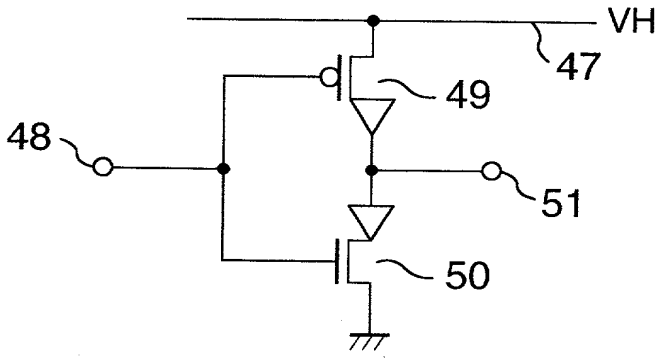


FIG.8

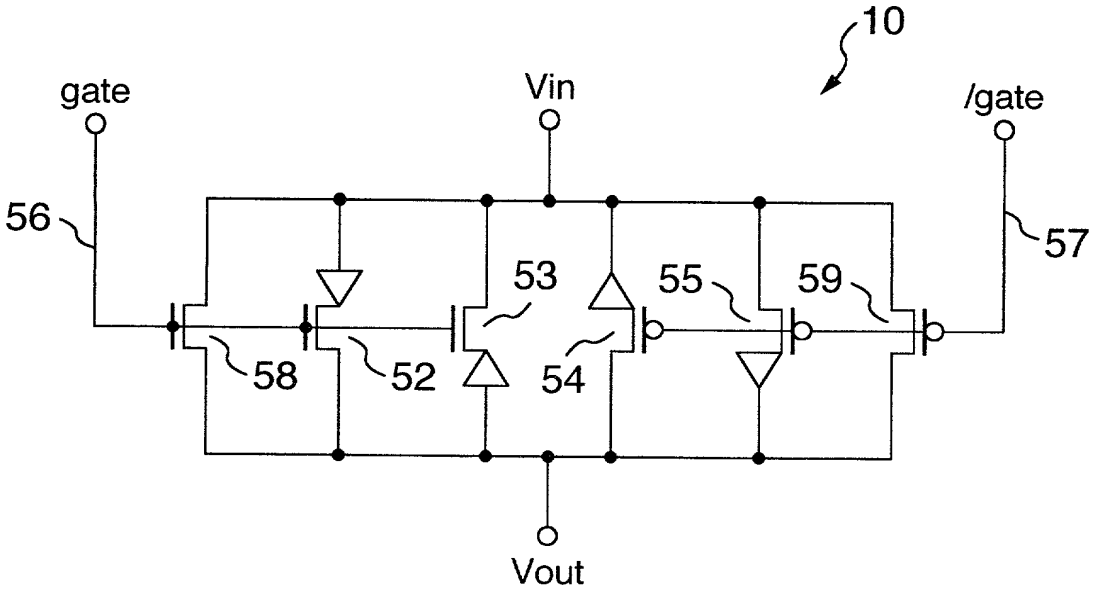

10
gate
Vin
/gate
56
57
53
55
59
58
52
54
Vout

FIG.9

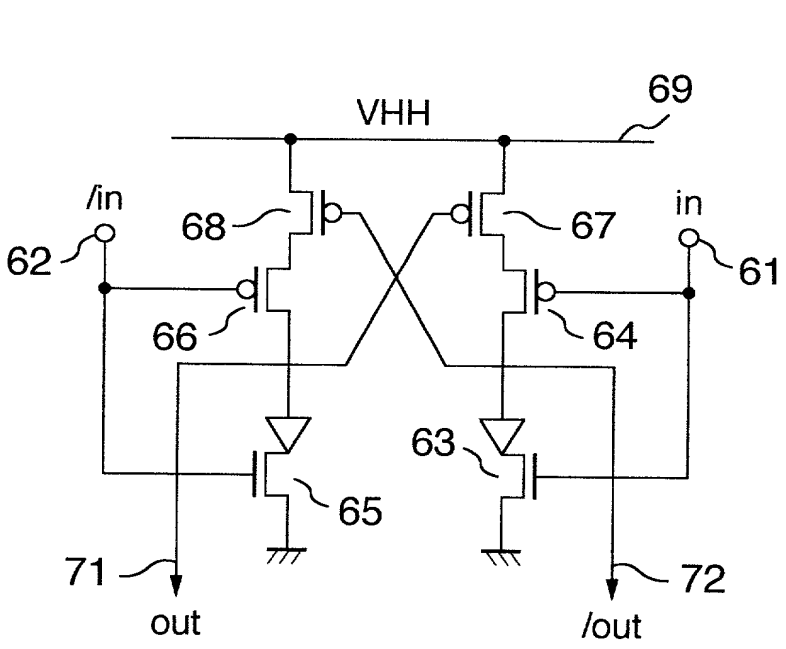

7
69
VHH
/in
68
67
in
62
61
66
64
63
65
71
72
out
/out

FIG.10

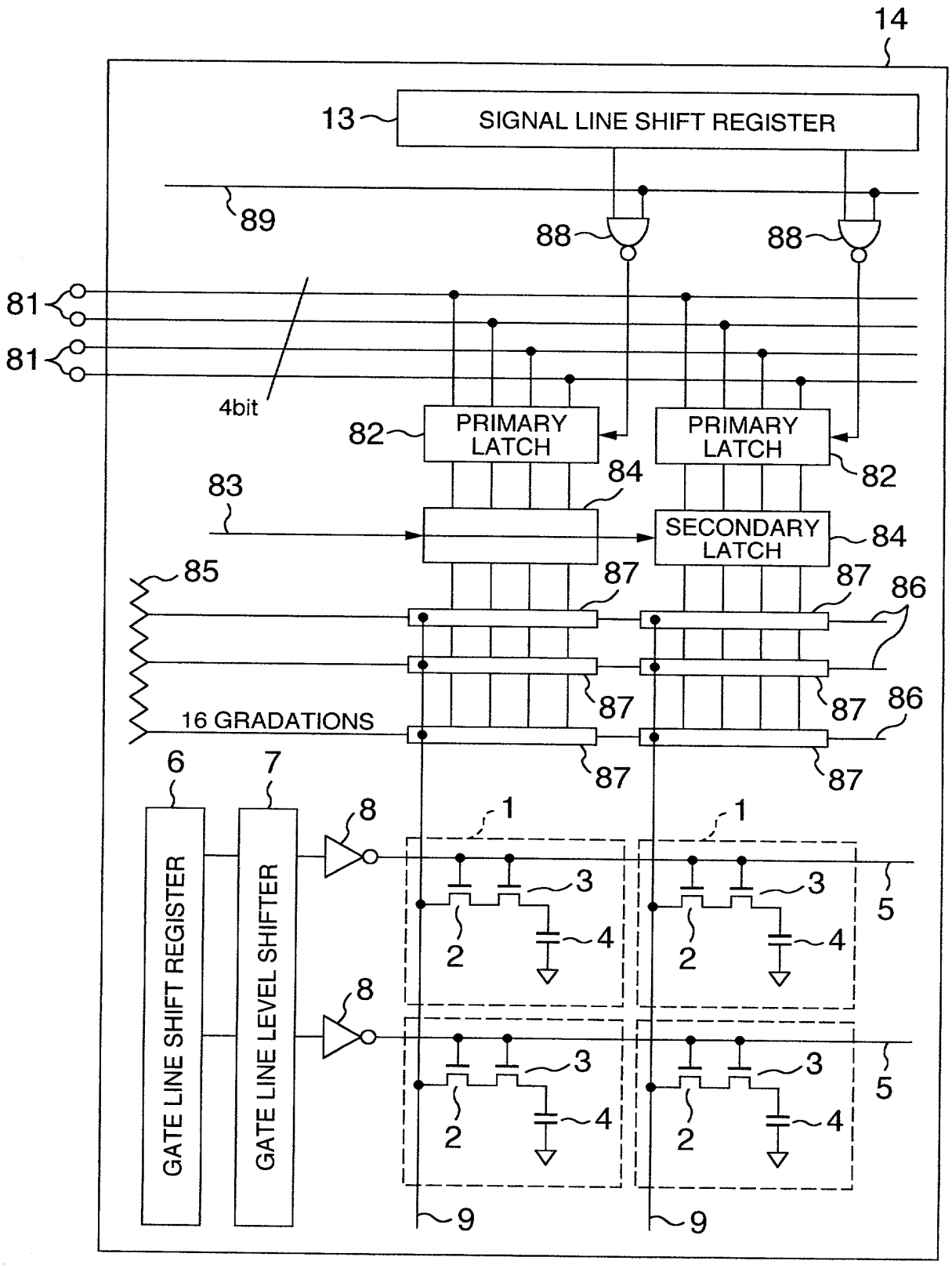

14
13
SIGNAL LINE SHIFT REGISTER
89
88
88
81
81
4bit
82
PRIMARY LATCH
PRIMARY LATCH
82
83
84
SECONDARY LATCH
84
85
87
87
86
87
87
86
16 GRADATIONS
87
87
6
7
8
1
1
GATE LINE SHIFT REGISTER
GATE LINE LEVEL SHIFTER
3
3
5
2
4
2
4
8
3
3
5
2
4
2
4
9
9

FIG.11

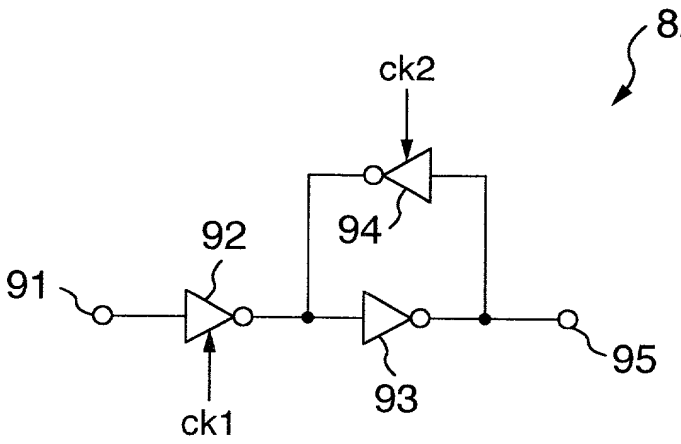


FIG.12

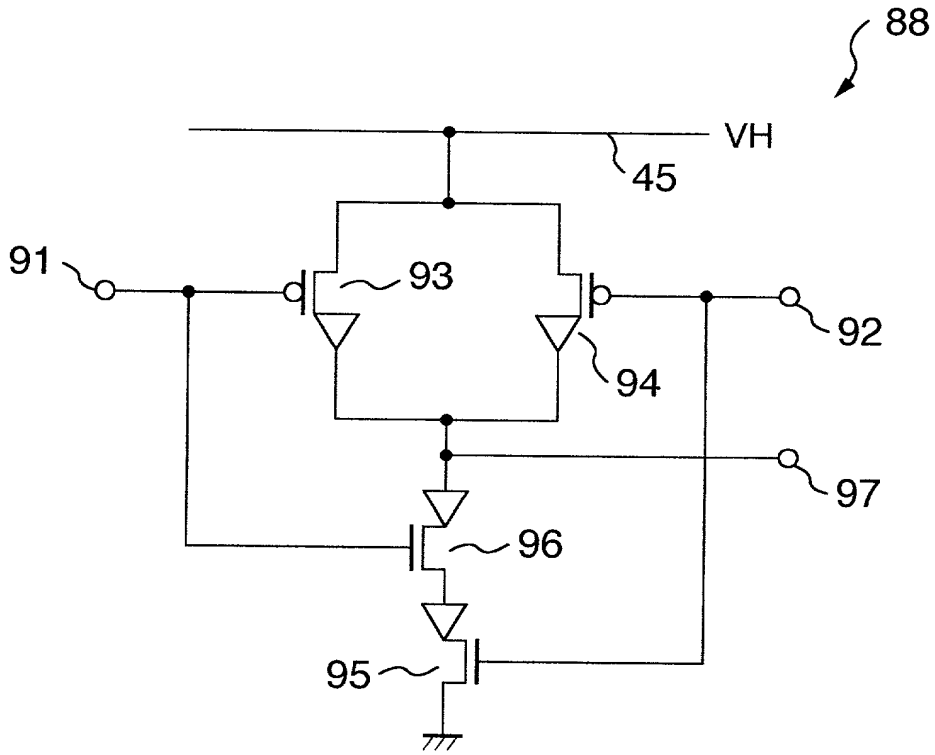


FIG.13

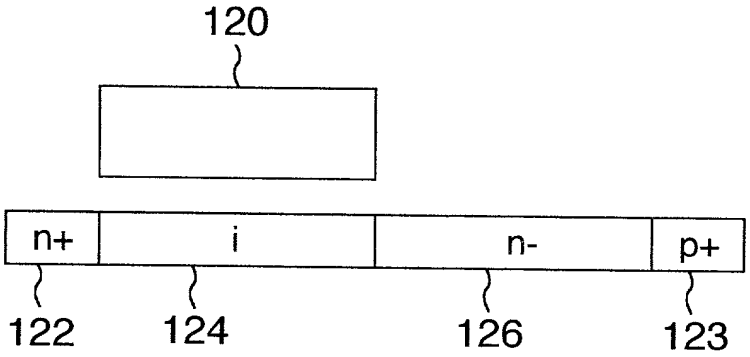


FIG.14

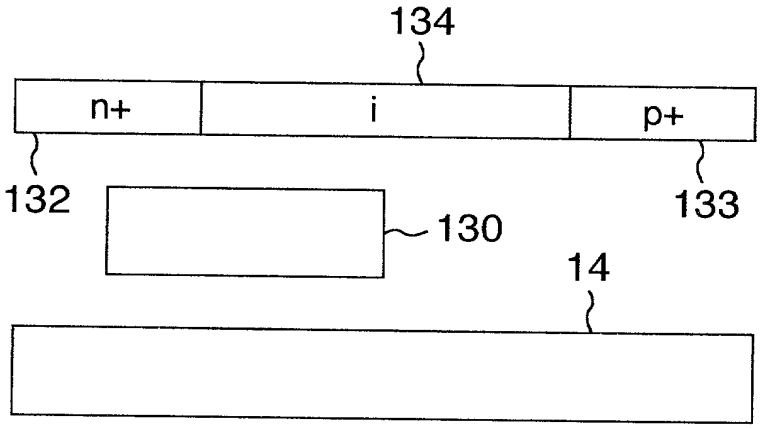


FIG.15

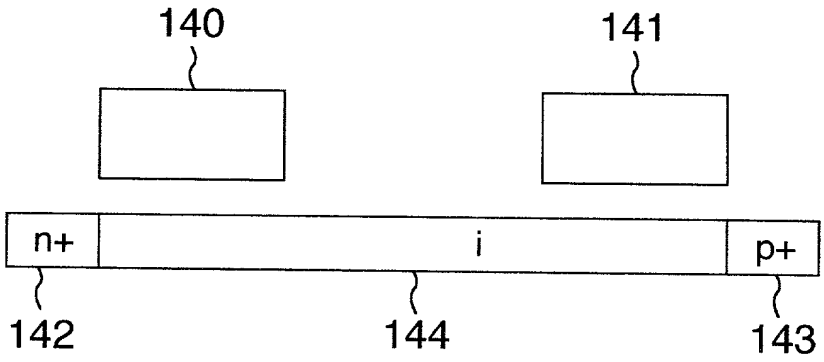

140
141
n+
i
p+
142
144
143

FIG.16

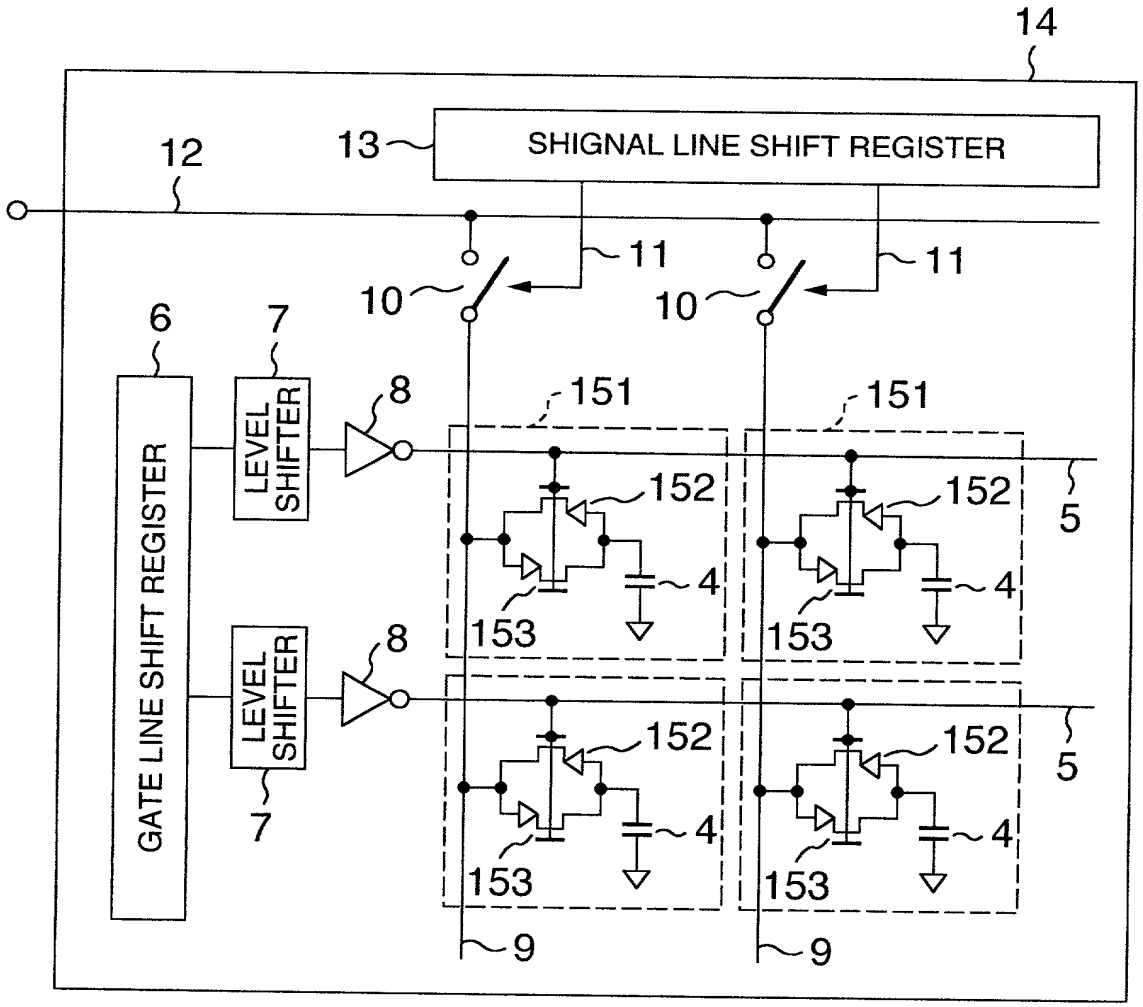

14
12
13
SHIGNAL LINE SHIFT REGISTER
11
11
10
10
6
7
GATE LINE SHIFT REGISTER
LEVEL SHIFTER
LEVEL SHIFTER
8
8
151
151
152
152
152
152
4
4
4
4
153
153
153
153
5
5
7
9
9

FIG.17

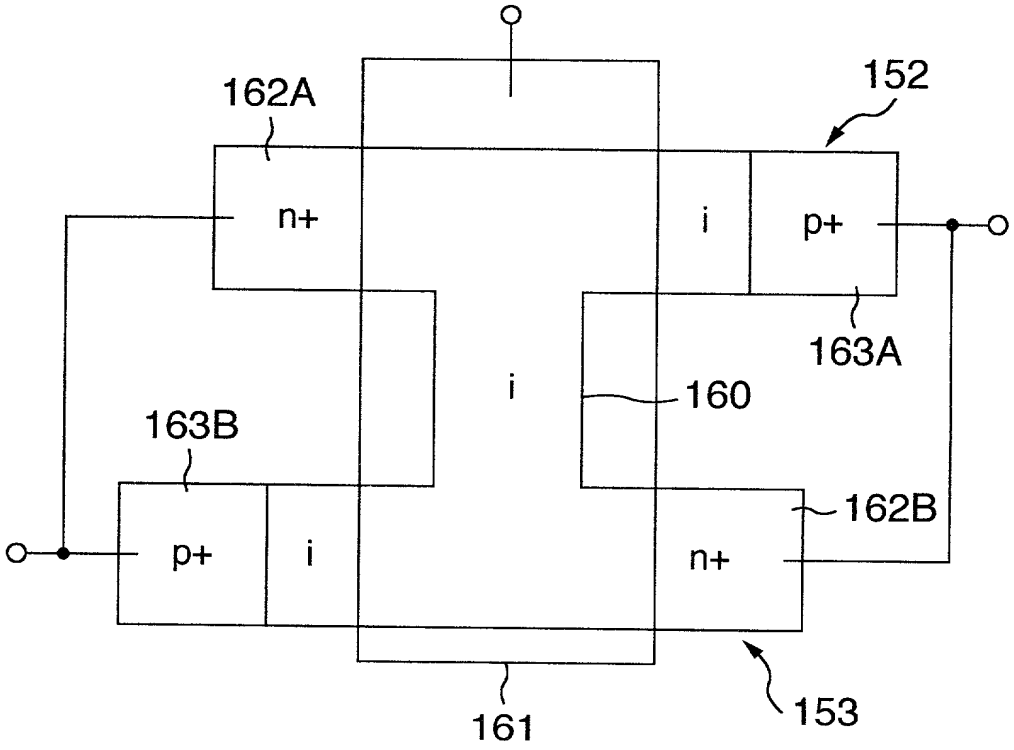

162A
152
n+
i
p+
163A
i
160
163B
162B
p+
i
n+
161
153

FIG.18

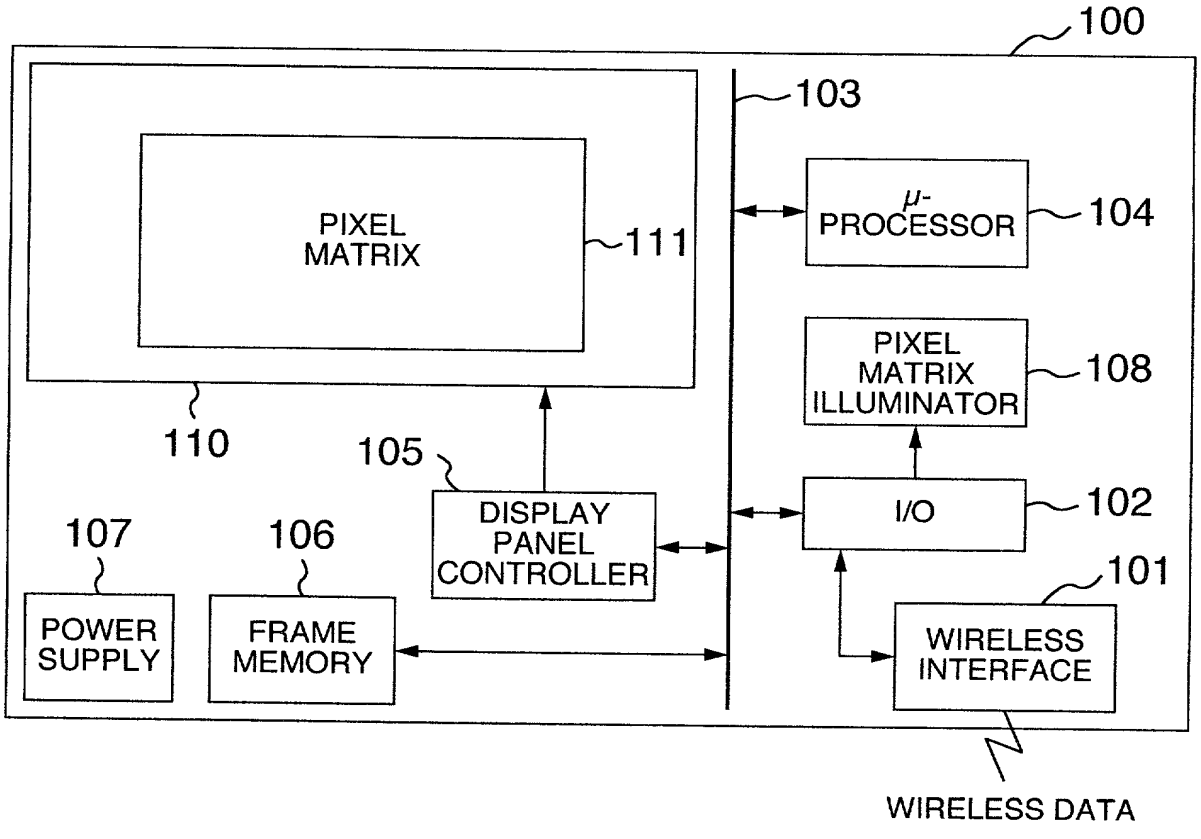

100
103
PIXEL MATRIX
111
μ-PROCESSOR
104
PIXEL MATRIX ILLUMINATOR
108
110
105
DISPLAY PANEL CONTROLLER
I/O
102
107
106
101
POWER SUPPLY
FRAME MEMORY
WIRELESS INTERFACE
WIRELESS DATA

FIG.19
(PRIOR ART)

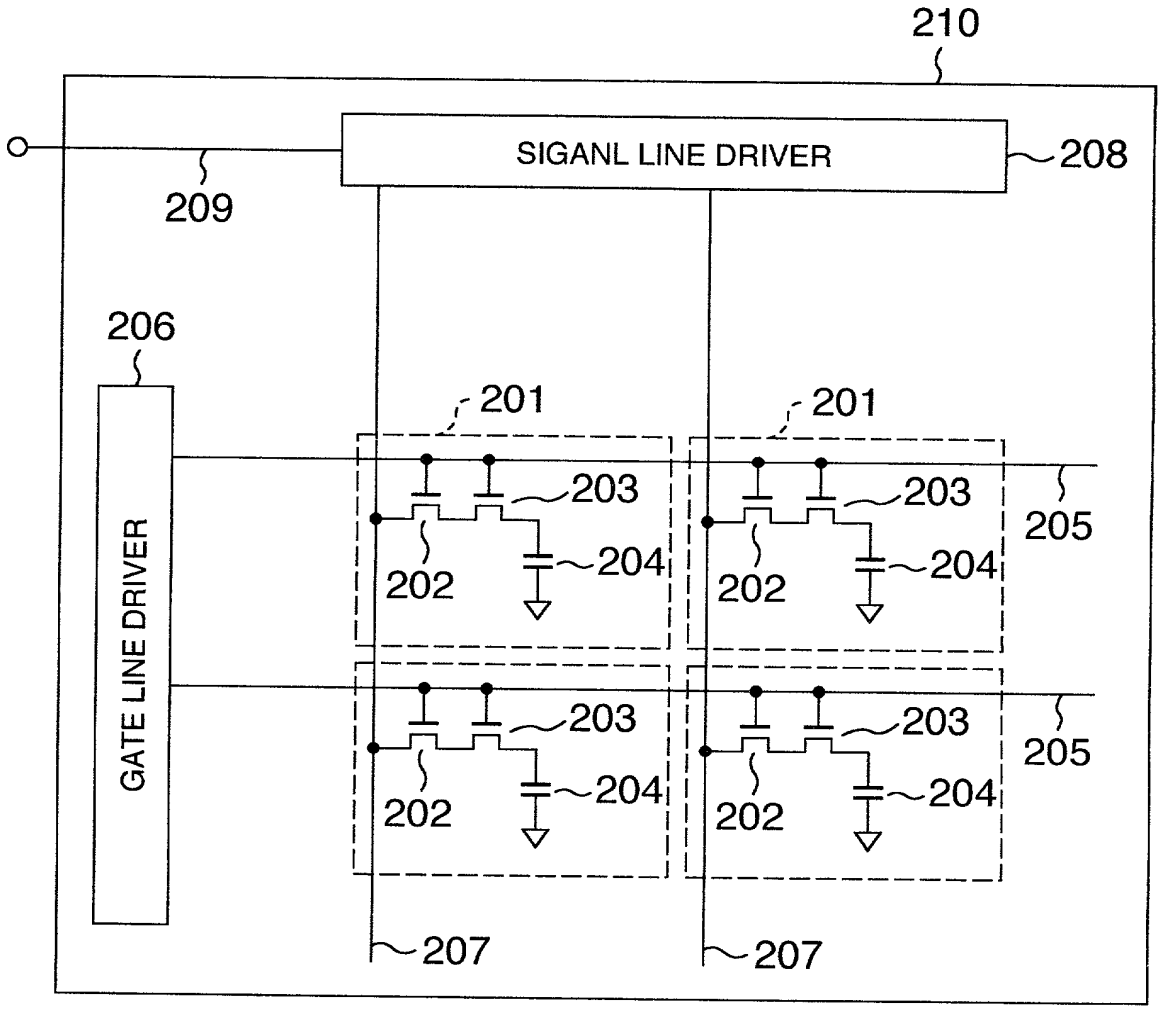
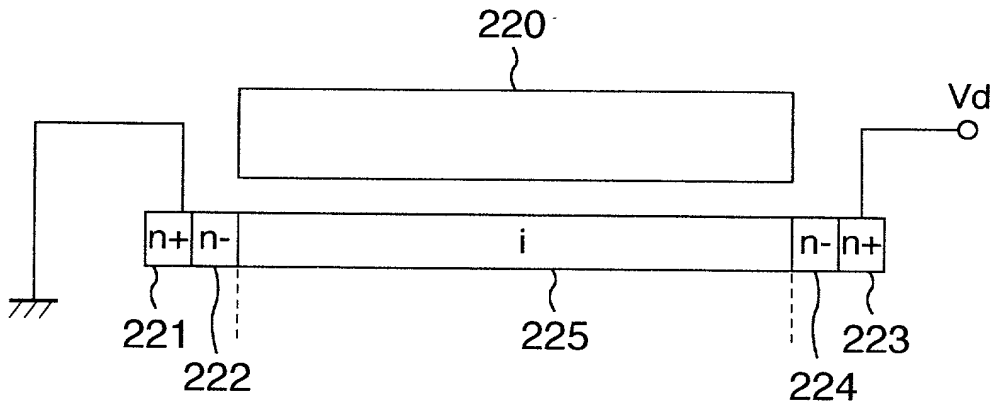
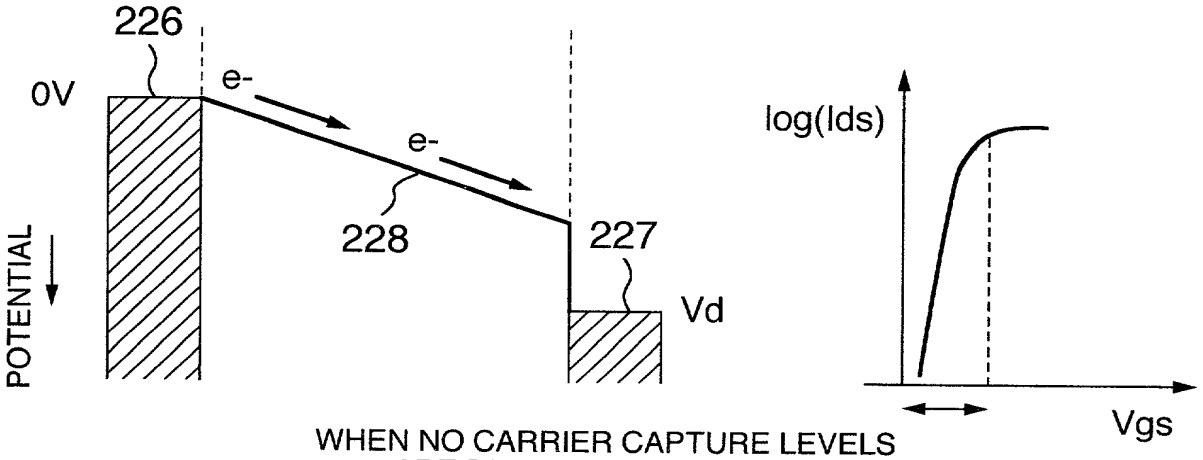


FIG.20A
(PRIOR ART)



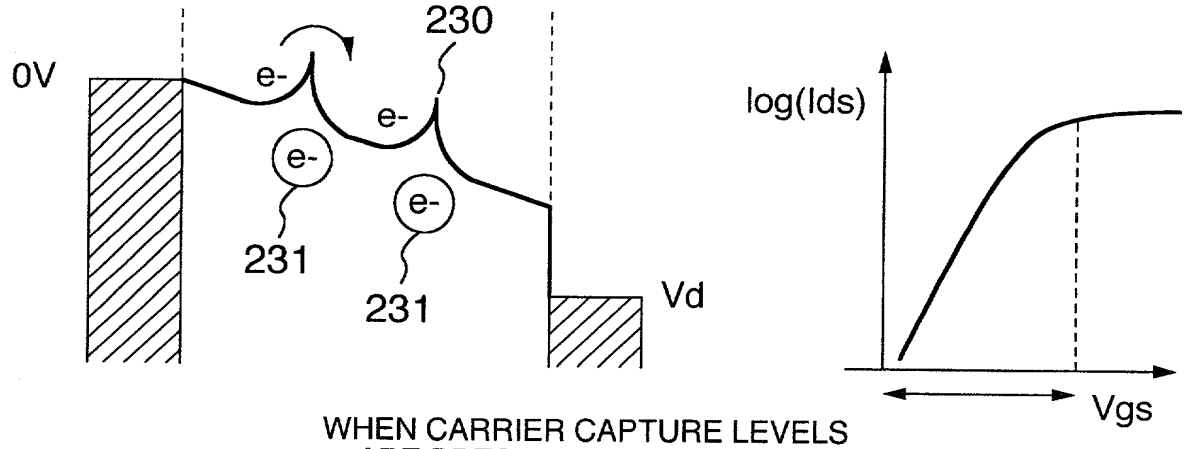
CROSS SECTION

FIG.20B



WHEN NO CARRIER CAPTURE LEVELS
ARE PRESENT(IDEAL CASE)

FIG.20C



WHEN CARRIER CAPTURE LEVELS
ARE PRESENT(ACTUAL CASE)